AMENDMENTS TO THE CLAIMS:

The following listing of claims replaces all prior listings, and all prior versions, of claims in the application.

LISTING OF CLAIMS:

Claims 1-22. (Canceled).

23. (new) A LSI comprising:

a central processing unit;

a memory controller for controlling a synchronous dynamic memory,

wherein said memory controller is operable to receive an access request from said central processing unit or said display unit to said synchronous dynamic memory having a data storage area divided into a plurality of banks, and

wherein said memory controller is operable to provide an active command for one of said banks to said synchronous dynamic memory, based on said access request,

wherein said memory controller is operable to provide a precharge command for another of said banks, which is to be accessed after said one of said banks, to said synchronous dynamic memory, said precharge command being provided after providing said active command, and

wherein said memory controller is operable to provide a read command or a write command for said one of said banks to said synchronous dynamic memory based on said access request,

wherein said read command or said write command for said one of said banks is provided after said precharge command is provided for said another of said banks.

24. (New) A LSI according to claim 23,

wherein data of said central processing unit is stored in said synchronous dynamic memory.

25. (New) A LSI according to claim 24

wherein said memory controller is operable to provide a RAS signal, a CAS signal, a WE signal and an address signal to said synchronous dynamic memory synchronized with a clock signal, and to provide said active command and said precharge command based on a predetermined combination of said RAS signal, said CAS signal, said WE signal to said external memory.

26. (New) A LSI according to claim 24,

wherein said memory controller is operable to provide address signals including a bank address signal, and a row address signal or a column address signal, to said synchronous dynamic memory synchronized with a clock signal.

27. (New) A LSI for processing comprising:

a central processing unit to execute data processing;

a display unit to output image data; and

a memory control unit operable to read access or write access to an external synchronous DRAM having a data storage area divided into a plurality of banks,

wherein said memory control unit is operable to receive an access request from said central processing unit or said display unit to said external synchronous DRAM; and

wherein said memory control unit is operable to provide an active command for one of said banks to said external synchronous DRAM, based on said access request,

wherein said memory control unit is operable to provide a precharge command for another of said banks, which is to be accessed after said one of said banks, to said external memory, said precharge command being provided after providing said active command,

wherein said memory control unit is operable to provide a read command or a write command for said one of said banks to said external memory based on said access request, and

wherein said read command or said write command for said one of said banks is provided after said precharge command is provided for said another of said banks.

28. (New) A LSI for processing according to claim 27,

wherein said memory control unit is operable to provide a RAS signal, a CAS signal, a WE signal and a bank address signal to said external memory synchronized with a clock signal, and to provide said active command and said precharge command based on a predetermined combination of said RAS signal, said CAS signal, said WE signal.

29. (New) A LSI for processing according to claim 27,

wherein said central processing unit is operable to access for read out of data stored in said external synchronous DRAM, and

wherein said display unit is operable to access read out data stored in said external synchronous DRAM.

30. (New) A LSI for processing according to claim 29,

wherein said memory control unit is operable to provide access signals, including a bank address signal and an address signal, to said external synchronous DRAM synchronized with clock signals.

31. (New) A LSI comprising:

a CPU to execute data processing;

a display processing unit to output graphic data; and

a memory controller to access to an external synchronous memory synchronized with clock signals,

wherein said memory controller is operable to receive an access request from said CPU or said display processing unit to said external synchronous memory, wherein said external synchronous memory includes a data storage area divided into a plurality of banks,

wherein said memory controller is operable to provide an active command for one of said banks to said external synchronous memory, based on said access request,

wherein said memory controller is operable to provide a precharge command for another of said banks, which is to be accessed after said one of said banks, to said external memory, said precharge command being provided after providing said active command, and

wherein said memory controller is operable to provide a read command or a write command for said one of said banks to said external synchronous memory based on said access request wherein said read command or said write command for said one of said banks is provided after said precharge command is provided for said another of said banks.

32. (New) A LSI according to claim 31,

wherein data of said CPU is stored in said external synchronous memory.

33. (New) A LSI according to claim 32,

wherein said memory controller is operable to provide a RAS signal, a CAS signal, a WE signal and a bank address signal to said external memory synchronized with said clock signals.

34. (New) A LSI according to claim 31,

wherein said memory controller is operable to provide a bank address signal and an address signal to said external memory synchronized with said clock signals.

35. (New) A LSI according to claim 23,

wherein data of said display unit is stored in said external memory.

36. (New) A LSI according to claim 23,

wherein said memory controller is operable to provide said precharge command, after receiving said access request from said display unit.

37. (New) A LSI according to claim 23,

wherein said memory controller is operable to provide address signals including a bank address,

wherein a bank address outputted with said active command is the same as a bank address outputted with said read command or said write command, and

wherein a bank address outputted with said precharge command is an address of said another of said banks to be accessed, wherein said read command

or said write command for said one of said banks is provided after said precharge command is provided for said another of said banks.

38. (New) A LSI according to claim 27,

wherein said memory control unit is operable to provide said precharge command, after receiving said access request from said display unit.

39. (New) A LSI according to claim 27,

wherein said memory control unit is operable to provide address signals including a bank address,

wherein a bank address outputted with said active command is the same as a bank address outputted with said read command or said write command, and

wherein a bank address outputted with said precharge command is a bank address of said another of said banks to be accessed after said one of said banks.

40. (new) A LSI comprising:

a central processing unit;

a memory controller for controlling a synchronous dynamic memory,

wherein said memory controller is operable to receive an access request from said central processing unit or said display unit to said synchronous dynamic memory having a data storage area divided into a plurality of banks, and

wherein said memory controller is operable to provide an active command for one of said banks to said synchronous dynamic memory, based on said access request,

means for permitting access to another of said banks, which is to be accessed after said one of said banks, even if a mishit occurs as to access to said one of said banks, said means comprising:

said memory controller being operable to provide a precharge command for said another of said banks, which is to be accessed after said one of said banks, to said synchronous dynamic memory, said precharge command being provided after providing said active command, and said memory controller being operable to provide a read command or a write command for said one of said banks to said synchronous dynamic memory based on said access request, said read command or said write command for said one of said banks being provided after said precharge command is provided for said another of said banks.